Integrated Circuits- Measurement of Electromagnetic Immunity

Conducted measurements

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Summary

1. Bulk Current injection method
2. Direct RF Power Injection method
3. Workbench Faraday Cage method
Integrated Circuits- Measurement of Electromagnetic Immunity

Bulk Current Injection method, 10 KHz-1 GHz
Bulk Current Injection (BCI) method

- Method for measuring the immunity level of IC to RF electromagnetic disturbance limited to continuous narrowband RF signal
- This method applies to IC that have any kind of connection to cable harnesses
- This test method can be used to inject current on one or more pins simultaneously to cause the IC malfunction
- The malfunction may be classified from A to D, according to the performance classes defined in IEC 62132-1
Measurement of Susceptibility

Inductive coils
Widely used in embedded electronics
Very similar to EM wave in Automotive
(DC-150MHz)
Inductive coupling to the network
Parasitic current injected on the chip, may alter CAN driver information and induce a fault inside the micro-controller
Limited to 400 MHz, due to the cut-off freq of the injection coil
BCI Examples
Bulk Current Injection method

**Coupling paths:**
- In systems: *cable harnesses*
- In pcb: *traces*

This method has good correlation with direct radiated RF immunity test results, especially at lower frequencies.
BCI, Hardware Test Set Up

- The fault is defined with a parameter called immunity criteria, which is checked with IC control system.
- This procedure is configuration dependent on their application: each pin or pins (ex. Balanced systems) that is expected to be exposed to external RF disturbances, should be tested individually.
BCI Test characteristics

- **Test conditions**: IEC 62132 Part 1
- **IC test plan**: document to precise specific test parameters:
  - Which pin/s should be tested and how: *separately or as a pair*
  - The immunity criteria used
  - IC Test set-up
- **Freq range**:
  - 10 KHz – 1 GHz
  - Changes: should be noted in Test Report
  - Upper freq determined by injection probe physical size
BCI Test characteristics

- **Test signal:**
  - According to IEC 62132-1
  - Non-modulated, CW
  - And/or AM signal (1 KHz, 80 %) with sufficient dwell time at each freq.

These type of signal waveform are used in automotive applications

Before applying the AM signal, with factor modulation $m$, the level should be set $20\log(1+m)$ dB down in respect to CW level

Ex.: for $m=80\%$ 5.1 dB
BCI Test characteristics

- **Freq. step size:**
  - According to IEC 62132-1
  - if another freq step is needed=> should be described in the IC Test plan
  - The choice should be cover all immunity range of IC and avoid skipping freq immunity.

  *In general IC disturbances root causes are due to impedance resonances. These are often very thin and the freq step should take account these phenomenon*

- There are 2 ways to define freq steps: *linear* or *logarithmic approach*

  Examples in automotive and aerospace applications:

<table>
<thead>
<tr>
<th>Frequency band</th>
<th>Maximum frequency size step</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 kHz to 100 kHz</td>
<td>2 kHz</td>
</tr>
<tr>
<td>100 kHz to 1 MHz</td>
<td>20 kHz</td>
</tr>
<tr>
<td>1 MHz to 10 MHz</td>
<td>200 kHz</td>
</tr>
<tr>
<td>10 MHz to 100 MHz</td>
<td>2 MHz</td>
</tr>
<tr>
<td>100 MHz to 1 GHz</td>
<td>5 MHz</td>
</tr>
</tbody>
</table>

*Linear* frequency step (a+a)  
*Logarithmic* frequency step (a)
Test Immunity Levels

- The test signal severity level is the test current of the calibrated test current applied.
- This test severity levels are expressed in terms of the equivalent RMS value of the unmodulated signal (from module testing)
- The levels applied at IC testing shall take into account the transfer function of the individual wires involved in relation to the cable harness

<table>
<thead>
<tr>
<th>Test Severity Level</th>
<th>Current (CW value) No insertion loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>50 mA</td>
</tr>
<tr>
<td>II</td>
<td>100 mA</td>
</tr>
<tr>
<td>III</td>
<td>200 mA</td>
</tr>
<tr>
<td>IV</td>
<td>300 mA</td>
</tr>
<tr>
<td>V</td>
<td>Specific value agreed between the users of this std.</td>
</tr>
</tbody>
</table>
Bulk Current Injection (BCI)

• The injection probe is a current transformer through the center of which each tested terminal or several terminal of the DUT are passed.
• The size of the injection probe determines the upper freq. to which the set-up can be used.
• Varying the test severity level and freq. of the induced disturbance carries out the immunity test.
Instrumentation

Generally specified in IEC 62132-part 1:

- Ground plane
- Current injection probe
- Current measurement probe
- Supply line load(s)
- High freq. Signal generator with AM & CW
- RF power amplifier
- Wattmeter to measure the direct and reflected power.
- Current measurement instruments
- Directional coupler and optical interface

Obs.: between 10 to 500 KHz the insertion loss of the probe (eg. 20 db/dec), should be taken into account.
BCI Test Set up (Ex)

- A set of probes capable of operating over the test freq range is required to couple the test equipment to the DUT measurement probe, or
- Set of probes capable of operating over the specified test freq range shall be terminated with the load impedance having the same value as used during the calibration
The disturbance is current \( I_{\text{disturbance}} \) flowing in a small loop comprising: wire(s), input impedance(s) of IC and ground – direct or via the feed-through capacitance (represented as the dotted lines on the left side of the fig).
Test PCB

- DUT is mounted on a **relevant PCB**
- The sizes of PCB designs are depending on the size(s) and construction(s) of the current probes.
- The test PCB (def in IEC 62132-part 1) can be taken which is either soldered or otherwise properly contacted with the overall test PCB
- The injection wire is connected to the IC pin(s) selected at one end and to the appropriated load, supply, or support circuitry at the other end.
- The injection wire length is limited at $\frac{1}{4} \lambda f_{\text{max}}$ of the test method (1 GHz)

**Advantage:** Fix the position of the probes

**More repeatable measurement!**
Test PCB fixture

• The PCB is placed on a copper test fixture connected to the ground system.
• The **Test PCB fixture** is used to avoid resonances in the ground system.
• It is recommended when large current probes need to be supported.
Support PCB fixture

The probe support shall be made from non-conductive materials.
Test procedure

• It is recommended to prepare an **IC Test plan** prior to perform the test:
  – Information on the electrical diagram
  – The applied stimuli representing disturbing signals
  – Acceptance criteria
  – In detail the test conditions

• The **Test plan** shall be included in the **Test Report**.
Test procedure

- A disturbing signal (RF current) is injected into the selected DUT pin(s) using closed loop feedback control to assure that the required forward power limit is not exceeded.
- The power limit is determined for applied disturbance freq during the calibration process, performed with the help of calibration fixture.

It is *preferable* to perform the RF immunity test in an enclose providing sufficient shielding conditions.
Calibration of forward power limitation

**Calibration fixture:**

- **Caution:** Use a load with an adequate power rating

The level of forward RF power (in CW mode) supplied to the injection probe is established, in order to generate the desired current $I_{\text{limit}}$. 

- Electrically short section of a transmission line
- Spectrum analyzer or RF voltmeter
Calibration of forward power limitation

**Calibration procedure:**

1. Connect the components of test equipment as seen in previous slide
2. Increase the amplitude of the test signal to the injection probe until the required current level, as measured by the RF receiver, is reached.
3. Record the forward RF power necessary to generate the desired current $I_{\text{limit}}$.
   This RF power is admitted as the maximum forward power limit $P_{\text{limit}}$.
4. Reduce the RF power before changing freq of the disturbance signal.
5. Repeat steps 2 to 4 for each freq step within the specified freq range.

The Calibration results shall be documented in the Test Report.
Detail Test procedure

- In the RF immunity test procedure a closed loop circuit is used, which allows keeping the RF power limit to $P_{\text{limit}}$ and the measured current.
- The immunity level of IC is found; when the RF immunity level is found.

Also the IC performance classes, and details regarding the RF immunity determination shall be recorded.
Test Report

• Shall be prepared in accordance with the requirements given in IEC 62132-1

• In all cases such parameters as:
  • Injected RF current I
  • Applied forward RF power P
  • Calibration power $P_{\text{lim}}$
  • Calibration current $I_{\text{lim}}$

  Shall be documented in the test report.
BCI measurement example

- Config 2 shows an improved behavior, meaning a lower sensitivity to injected parasitic sinusoidal wave.
- This spectacular improvement is done by appropriate filtering, protection, careful PC, package and IC floorplan routing.

Typical circuit which exhibits a susceptibility weakness from 200 to 800 MHz
Integrated Circuits - Measurement of Electromagnetic Immunity

Direct RF Power Injection method,
150 KHz-1 GHz
Introduction

• This is *a method to measure the immunity of IC* in presence of conducted RF disturbances, eg. *Resulting from radiated RF disturbances*

• This standard *establishes a common base* for the evaluation of semiconductor devices used in equipment, which works in an environment, which is subject to unwanted RF electromagnetic waves.

• This method *guarantees* a high degree of *repeatability* and *correlation* of immunity measurements.
Measurement basics

An IC gets the unwanted RF energy through those pins connected to wires (cable harness and/or traces of a PCB), which may be efficient antennas.

Therefore, the electromagnetic Immunity of an IC can be characterized by conducted RF –disturbances (i.e.: RF forward power) instead of field parameters as it is usually done in module and/or system testing.
Measurement basics

- For module or system test, the forward power provided to circuit by the cable harness or traces on PCB acting as antennas can be measured or estimated, no matter whether it will be reflected or absorbed.

- It has been observed that many ICs are most susceptible to the disturbances at quite high reflections (*highest values*)

- To characterize the immunity of an IC the forward power needed to cause malfunction is measured

- The malfunction may be classified from A to D according to IEC 62132-1
Hardware Test Set-up

[Diagram of hardware test setup with components labeled: DC supply, 50 Ohm coax, directional coupler, RF amplifier, RF generator, RF Power meters, test PCB, decoupling network, DC Block, RF injection port, DUT, optional control PC, and DUT monitor.]
DPI Set-up example
General Test Set-up

• Any function inside an IC can be affected even if it is not connected to the pin under test. Therefore the operation mode(s) of the IC shall be chosen in a way that all functions of the IC are used during the test.

• ICs are often used in different configurations based on the application:
  – In order to understand the influence of each individual pin, each pin that is expected to be exposed to RF disturbance should be tested individually.
  – Multiple pin testing is permissible into pins of differential mode systems.
System and IC parameters affecting immunity of a pin

<table>
<thead>
<tr>
<th>IC related parameters</th>
<th>module related parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>circuit design</td>
<td>protection of the pin by external components</td>
</tr>
<tr>
<td>chip layout</td>
<td>operation mode of the IC</td>
</tr>
<tr>
<td>ground system inside the IC</td>
<td>ground system</td>
</tr>
<tr>
<td>pinning and bond design</td>
<td>board layout</td>
</tr>
<tr>
<td>package</td>
<td>impedance of wiring harness and load</td>
</tr>
<tr>
<td>technology</td>
<td></td>
</tr>
<tr>
<td>circuitry connected to a pin</td>
<td></td>
</tr>
</tbody>
</table>

Knowing the immunity of an IC (the highest forward power that does not affect the function of the IC) allows the user to decide if he needs external protection means and how much effort has to be spent for external protection.
Single pin direct power injection

- **C** may be used as a DC block. Default value=6.8 nF (as specified in IEC 61967, part 4)
- **R** may be used for current limitation or to simulate a load of a real application. Default value=0 Ω, up to 100 Ω (if functionally required)
  - When R=0 Ω each input or output of the DUT will be loaded by the 50 Ω of the RF per injection system.
- Chosen **R** and **C** values shall be stated in the **Test Report**
Multiple pin direct power injection into pins of differential mode systems.

If two or more pins are used to transfer information as differential mode signal in analogue or digital form, then multiple pin direct RF power injection can be used to test the common mode immunity.
Test conditions

- **General test conditions**: IEC 62132-part 1
- **Test levels of the forward power**: depend on the application of the DUT and the pin that is being tested.
  - Max CW RF-signal for testing an externally:
    - unprotected IC-pin = 5 W (37 dBm)
    - protected IC-pin= can be decreased in “protective zones”:

Example of a specification of immunity level ranges e.g. for automotive applications

<table>
<thead>
<tr>
<th>Zone</th>
<th>power (Watt)</th>
<th>device externally protected by</th>
<th>example for devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1 ... 5</td>
<td>nothing or only a small capacitor as filter</td>
<td>high side switches, power supply circuits, Bus-transceiver for driving wire harness (e.g. CAN, LIN)</td>
</tr>
<tr>
<td>2</td>
<td>0.1 ... 0.5</td>
<td>L-,R-,C-low pass filter</td>
<td>signal conditioning devices, ABS sensor circuit, communication line driver</td>
</tr>
<tr>
<td>3</td>
<td>0.01 ... 0.05</td>
<td>no direct connection to the environment, decoupling by placing</td>
<td>Microcontroller, memories</td>
</tr>
</tbody>
</table>
Test conditions

• *Signal:*
  – CW and/or AM as agreed by the users
  – By default: AM, 1KHz 80 %
  – If other modulations are used, they shall be stated in the **Test Report.**
  – When AM signal is used the peak power shall be the same as for CW.
Test equipment

• **Specified in General:** IEC 62132-part 1

• **RF power source:**
  – RF generator
  – RF power amp:
    • provide sufficient power even into a mismatched load (recommendation: use higher power capability (max. level 5 W => max power 10 – 50 W))
    • Output impedance 50 Ω (recommended: VSWR < 1,2), if not an attenuator for matching shall be placed before the transmission line.
    • Spurious emission ≤ 20 dB carrier level.

• **RF power meter and directional coupler:**
  – VSWR < 1,15 in the applicable freq range.
  – It is recommended to use a power meter with peak envelope measurement capability for power measurement during modulation.
Test set-up

- Power injection set-up consists of 2 parts:
  - *The first part is not on the test board:*
    - A RF power source (RF gen., amp., *attenuator*)
    - Coaxial cables
    - RF connectors
    - A directional coupler with measuring head for forward power
  - *The second part is placed directly on the testboard:*
    - RF injection port to connect the coaxial cables and the transmission line on PCB
    - The connection from the end of the transmission line (RF injection port) via the DC block to the DUT
    - DC biasing networks connected to the pin under test.

Power reflected by the DUT should not be reflected to the DUT again by an impedance discontinuity somewhere else in the power injection set-up.
Test set-up

• Test circuit board:
  – *Strongly recommended:* Use of a PCB with common RF ground plane for immunity testing of ICs.
  – The DUT should be placed on the test board without sockets because most sockets have significant inductance that will affect the test (for instance $10\text{nH @ 1 GHz} \Rightarrow X_L = 63 \ \Omega$)
  – It is the main purpose of this standard to test the immunity of the DUT only. *Therefore, all external protection components of the DUT shall be removed unless it is absolutely mandatory to have these external components to achieve proper function on the IC (blocking capacitors, timer capacitors, etc.).*

Such mandatory blocking shall be placed directly at the IC and be regarded as if it would be part of it. They shall be grounded on the same ground plane. Return paths from mandatory blocking components to the DUT or the shield of a transmission line should not have slits.
Example of the routing from the injection port to a pin of the DUT

- **Target:** Trace lengths and return paths $\leq 1/20 \lambda_{\text{min}}$
- The impedance between the DUT ground pin(s) and the shield of any transmission line providing the RF signal shall be as low as possible. Therefore using a ground plane on PCB to minimize the impedance of ground connections is strongly recommended.

For cases where it is not possible to follow these “rules” the used power injection set-up shall be characterized and documented in the **Test Report**.
Hints for the best installation (I)

**Basic approach**: is to carry the RF to be injected as close to the DUT as possible without leaving the 50 Ω transmission line system.

**a) ICs with a low number of pins**

Using a board as small as possible and placing the connector of the transmission line as close to the device as possible.

- **Coax-cable connector placed on the board nearby the DUT**

- **Using a shield box placing the connector as close as possible to the DUT (optional series resistor may be added)**
Hints for the best installation (II)

**Basic approach:** is to carry the RF to be injected as close to the DUT as possible without leaving the 50 Ω transmission line system.

**b) ICs with a high number of pins**
- Using a large board implementing traces on the board that are transmission lines with an impedance of 50 Ω to keep the total VSWR < 1,2.
- Jumper fields within the microstrips should be avoided in order not to get impedance discontinuity, which causes multiple reflections (resonance)
- The test set-up may consist of a general strip line board and an IC specific application board on top of it.

Accessing a high pin count DUT by a large main board and an IC specific board connected by spring contact pins
Characteristics of the power injection set-up

To characterize the power injection set-up:

Replace the IC by a proper 50 Ω system and measure the S21 parameter from the RF injection port to the pad of the specified IC pin in a 50 Ω system. The S21 parameter must have a constant behavior over the used frequency range without any resonance. A max tolerance of 3 dB is possible.

Example of a S21 magnitude measurement result

(1st resonance above 1 GHz)
Decoupling networks

1. To supply the DUT at the pin that is submitted to the RF and to measure DC performance of the DUT while RF is applied a DC biasing network shall be used.

2. Other functional or aux signals should be connected via decoupling networks

**Characteristics:**
- Impedance $\geq 400 \, \Omega$ @ test freq. DC resistance depends on the requirements of the application (may be a single Resistor)
- The DC biasing network may also be connected to the injection path offside the PCB
- To minimize the effect of mismatching: path $< \lambda/20 \, f_{\text{max}}$ (e.g. $< 15 \, \text{mm}$ for 1 GHz)

*Coupling decoupling networks (CDN).*-Example: For common mode injection into differential mode signal lines as Asymmetrical Artificial Network (AAN or T-network) => CISPR 16-1

Obs. Depending on the application the impedance of such network may deviate, from the recommended $\geq 400 \, \Omega$ but shall be stated in the Test Report.
DC biasing and probing networks (I)

May consist of several coils and/or inductors in series with the one with the lowest L closest to the DUT.

Test set-up Example with the load on the test set-up.

The output is submitted to the RF disturbance and monitored for proper function at the same time. The high current flowing through the load does not need to be decoupled by an inductive filter.
DC biasing and probing networks (II)

If possible the same capacitor should be used as in the real application.

Test set-up with mandatory blocking capacitor

Note: The blocking capacitor in the test set-up should be on the same side of the PCB as in the real application.
DC biasing and probing networks (III)

Example of a decoupling network for an input with high impedance

Inputs with high impedance can be biased via a resistor

Termination of pins not to be tested with a typical impedance to reproduce crosstalk currents

Example of a decoupling network for an input with high impedance
DC biasing and probing networks (IV)

Example of power injection into a transceiver IC for differential data buses:

[Diagram of power injection network]
Test procedure

- The recommended default power level step can be 0,5 dB
- Default freq steps and dwell time are defined in IEC 62132-part 1
- To reduce the total duration of a test run for a highly immune DUT:
  - **Start from low levels** e.g. 20 dB below the forward power level specified for the test
  - Each power level shall be kept long enough to allow the IC to react (e.g. timer functions)

In accordance with the requirements of IEC 62132-part 1
A Test Report shall be prepared in accordance with IEC 62132-1.
IC - Measurement of Electromagnetic Immunity

Workbench Faraday cage method, 150 KHz - 1 GHz
Introduction

• The measurement procedure describes a measurement method to quantify the RF immunity of *ICs mounted on a standardized test board or in their final test board (PCB) application*, to *electromagnetic conductive disturbances*.

• This part applies to ICs that can perform “stand-alone” functions when used on a physically small test board

• This method makes it possible to classify ICs for dedicated functions where EMC constraints are applicable.

Examples:

– ICs used with cordless telephones,
– other communications devices,
– automotive,
– process measurement & control equipment,
– Product that control critical functions
Measurement philosophy (I)

• The workbench is derived from the IEC61000-4-6 publication
• This method has been proposed by Philips (and standardized under reference IEC 62132-5).
• It’s also used in emission measurements.
• The connected cables will have functions such as supply, communication and other signal interfaces and these cables are commonly not geometrically oriented in the same plane as the other cables
• The antennae (common-mode) impedance per port has been normalized to 150 Ω with tolerances in the various freq band. By injecting either a voltage in series or a current through these common-mode impedances, the RF immunity test is established.
• Due to the fact that induced currents will flow through the reference of the test board, indirect coupling between the voltages and currents through the package are also established.
Measurement philosophy (II)

• The workbench method shows the effect of the test board layout, the IC supply decoupling, the RF performance of the used discrete components (capacitors, inductors) as well as the measures taken on the IC (e.g. on-chip decoupling, filtered inputs and Schmitt-triggers used, etc.).

• The workbench method can be used for either absolute or comparative testing of ICs, either on the predefined, standardised test board, as well as for the measurement of definitive applications including ICs.

• In addition:
  – Similar modes of operation (by software or function) shall be used for the various ICs to be tested to allow comparison.
  – Various modes of operations with one IC allow comparison, i.e. determination of contribution of individual blocks within the IC.
General set-up

With common-mode impedances defined by using the CDN.
Workbench concept

• A small Faraday cage is used.
• Discrete resistors connected to several common-mode ports or the test board, i.e. test board are implemented to represent the coupling.
• The decoupling of supply and/or other I/O lines takes place via inductances build on ferrite cores representing impedances $>> 150\Omega$ @ freq of interest and feed-through filters installed through the wall of the cage.
Test conditions

• The test conditions shall be as described in IEC 62132-1

• When measurement are carried out using a test board other than defined in IEC 62132-1, that test board shall be described such that repetition of the measurement remains possible.

• When necessary a copy of the layout and circuit diagram shall be added to the Test Report.
Test equipment

- Meet the requirements as described in IEC 62132-1

**Test generator:**
- *RF generator* capable of covering the whole freq range of interest, and or being AM modulated by 1 KHz sine wave, 80 %. It shall have an automatic sweep capability and/or manual control
- *Attenuator T1* (typically 0 - 40 dB) of adequate freq rating, to control disturbing test source level. (T1 may be included in the RF generator)
- *RF switch S1* is used to switch the disturbing signal during immunity testing. (T1 may be included in the RF generator and is optional)
- Power amplifier (PA): appropriated bandwidth, distortion ≤20dB amplitude of the carrier level.
- *Appropriated filters* should be used to suppress harmonics or sub-harmonics of the RF generator or RF power amp.
- *Low-pass/high-pass filters* shall be applied when necessary, to prevent interaction of functional signal with the measured voltages. The applied filters shall be described in the Test Report
- *Attenuator T2* (fixed at 6 dB, Z₀ = 50Ω) with sufficient power rating. T2 is provided to reduce the mismatch from the generator or power amp (50Ω) to the coupling devices (150 Ω). T2 shall be located as close as possible to the coupling device. (T2 may be included in the coupling device and can be left out if the output of the signal generator remains within the specs under the given load condition)
The workbench Faraday cage is a shielded set-up. Required effectiveness ≥ 40 dB over a range of 10 MHz to 1 GHz. No additional shielding will be necessary.

- The inside of the box is covered with an anti-static insulating material to avoid a short of the test board toward the cage.
- An insulating support shall be used to support the test board under test or the test board as described in IEC 62132-1, in order to maintain the measuring height at 0.03 m.
Set-up for RF immunity testing using the WBFC

- The test generator shall be connected to the injection ports successively.
- In turn, the test board shall be rotated over 90°, where after the two measurements shall be repeated again.
- The worst-case reaction (detection, jitter, DC-offset) of the EUT shall be registered and a photo showing the set-up may be added to the Test report.

Ferrite rings: High common-mode impedance (ZL_CM=300Ω @ 150 KHz) between the test board and the reference (wall/bottom) of the cage.
Common-mode points

The number of common-mode points: 2, 3 or 4, which are used shall be recorded in the test report. As this number will influence the measured result substantially, an error of 4 dB is estimated between applications where 2 or 4 ports are terminated.

A set-up with only 2 ports connected while all other connections are left open or decoupled by using the ferrite cores is recommended.
150 Ω Network: Common mode impedance

Transmission line with $Z_o=150\,\Omega \pm 50\,\Omega$

Details of 4 resistors connected to wire mesh. Resistors shall be non-spiralized, metal film with a diameter of 6 mm typical. They extend the typical structure set by the 13 mm wire mesh.
150 Ω Network calibration

- Similar to the method described in IEC - 61000-4-6
- The common-mode impedance established by the transmission-line and the matching network can be measured
**Theory of Workbench method**

**WBFC lumped elements model**

- **E** coupling between the test board and the workbench cage

- **H** coupling between areas on the test board or between the IC and the test board may interact with the loop area formed between the workbench cage walls and the common-mode impedances \(Z_{cm}\) at both sides of the test board.

150Ω transmission-line & resistive network + external 50 Ω impedance (output RF disturbance generator, or a 50 Ω terminator)

A voltage may occur across the test board due to signal and supply currents running through the reference plane (Vss) resulting in a voltage drop across the plane (common impedance coupling), represented by the two (in-)dependent noise sources.
Test board

Depending on the purpose of the measurements, different kind of test boards can be used:

– **Pre-compliance testing.** Every test board can be used, as long as the separation from the edge of the test board to the walls of the cage is 0,06 m or more.

– **Absolute comparison.** The test board shall be as described in IEC 62132-1
Test procedure

• In accordance with the requirements of IEC 62132-part 1

• The test shall be performed with the test generator connected to each port in turn, while a 50 $\Omega$ resistor terminates all other ports of the coupling/decoupling devices.

• For comparison testing using the standardized test board, it’s advised to use two common mode points connected opposite to each other. Both ports shall be measured with the spectrum analyzer or selective volt and the max measured values at each freq shall be recorded (max-hold position).

• The test board shall be turned over 90° and two measurements with the analyzer still in max hold shall be repeated again. As such a worst-case measurement is carried out.
Immunity levels

• As various countries and product families may set different limits, no strict immunity limits or performance criteria can be given
• **Test Level:** Open-circuit test generator voltage levels (EMF) of the unmodulated disturbing signal ($V_{RMS}$):

<table>
<thead>
<tr>
<th>Level</th>
<th>Voltage level (EMF)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$U_0$ [dBµV]</td>
</tr>
<tr>
<td>1</td>
<td>120</td>
</tr>
<tr>
<td>2</td>
<td>130</td>
</tr>
<tr>
<td>3</td>
<td>140</td>
</tr>
</tbody>
</table>

| X *)    | Special |

*) X is an open level

• For comparison testing, these levels shall be followed, unless otherwise agreed between manufacturer(s) and customer(s)
• The IC under test shall be exposed to each level in turn until all levels have been tested or until immunity is identified. The level and freq at which an immunity is identified shall be noted in the Test Report.
Requirements for the WBFC test

• The following aspects shall be stated accurately:
  a) The orientation of the test board
  b) The number and position(s) of common-mode points
  c) The type and position of the peripheral connections to the test board (power supply, signals)
  d) The type of the applied filtering and peripheral cabling
  e) The type and number of the common-mode chokes used.

• The measuring instrument shall record the max measured response of the DUT at each freq. (max-hold position).

• The RF injection ports shall be interchanged at each port in turn, such that the total worst-case response (highest level) to all ports is measured.
Test results and test report

- The test report shall be as described in IEC 62132-1, specifically in accordance with chapter 9.
- The test report shall contain all specific requirements.
- When possible, a photograph of the set-up shall be made and added.
- **Immunity criteria**: depend strongly on the purpose of the measurement (*comparison of ICs* or *pre-compliance testing*), the application area and country, as RF immunity requirements may differ.