Abstract of course "Parameter Variations and Leakage in Nano-scale Technologies: Error Resiliency and Low-Power Design Methods" by Kausik Roy

In sub-50nm technologies, parameter variations and leakage currents are becoming one of the major issues. In order to have robust operations, there is a need for error resiliency under parameter variations. Unfortunately, error resiliency has conflicting requirements with low-power design requirements. In this talk, I will present voltage over-scaling as a means of lowering power dissipation and will consider several design methodologies at different levels of design abstraction (circuits, architecture, and algorithms) to achieve error resiliency under voltage over-scaling. It will be covered logic, memory, and signal processing applications.