Performance Analysis of a Clock Generator
PLL under TID Effects

Alan C. J. Rossetto; Ricardo V. Dallasen & Gilson I. Wirth
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Outline

• Introduction
• Review of Radiation Effects
• The PLL Circuit
• Case Study Circuit
• Methodology
• Results
• Conclusions
Introduction

- Electronic devices and circuits when exposed to radiation environment can suffer degradation in its electrical parameters
- This degradation affects the circuit performance and can cause functional failures
- This work analyzes the influence of TID in the performance of a clock generator PLL
- So, why a PLL?
  - Most of synchronous digital IC’s are controlled by a periodic signal – the clock signal
  - PLLs are the widespread topology for clock signals generation
  - An alteration/failure in the PLL can be propagated to whole circuit
Review of Radiation Effects

- Radiation exposure causes changes on the characteristics of electronic devices and circuits
- These changes may result in parametric degradation and/or functional failures
- In general, radiation effects can be divided in
  - Cumulative Effects: accumulation of defects in the device structure due to the incidence of ionizing or non-ionizing particles
  - Single Event Effects: are caused by a high energy particle strike in a sensible region of the device/circuit
- Cumulative effects can also be divided in
  - Displacement Damage (DD): result from the damage in silicon crystalline structure
  - Total Ionizing Dose (TID): result from the ionization of the semiconductor
• TID effects are result from the interaction between ionizing radiation and the dielectric structures of the devices
• It is usually caused by low energy particles
• Causes degradation of device electrical parameters due to charge trapping in the dielectric layers and in the interface silicon/oxide
• TID effects results in:
  • Threshold voltage shifts
  • Carrier mobility reduction
  • Leakage current increase
  • Flicker noise increase
PLLs are the widely topology for clock synthesis in digital IC’s

A PLL can be described as four essential blocks:
- A Phase-Frequency Detector – PFD
- A Loop Filter – LF
- A Voltage Controlled Oscillator – VCO
- A Frequency Divider – DIV

\[ f_{\text{CLOCK}} = N \cdot f_{\text{REF}} \]
The PLL Circuit

Basic Blocks

Function of Blocks

• PFD: Compares the phase and frequency difference between two periodic inputs, generating an error signal
• LF: Converts the current pulses from charge-pump in a voltage level in order to control the VCO
• VCO: Uses a voltage level to generate an output frequency
• DIV: Generates a feedback signal with lower frequency than the output, in order to achieve frequency multiplication
How does a PLL works?

- The PLL needs a reference frequency $f_{\text{REF}}$
- The PFD compares $f_{\text{REF}}$ against $f_{\text{FB}}$, generating $V_{\text{UP}}$ and $V_{\text{DN}}$ error signals
- If the $f_{\text{FB}}$ is slower than $f_{\text{REF}}$, the PFD triggers $V_{\text{UP}}$, in order to increase $V_{\text{CTRL}}$ and $f_{\text{CLOCK}}$
- If the $f_{\text{FB}}$ is faster than $f_{\text{REF}}$, the PFD triggers $V_{\text{DN}}$, in order to decrease $V_{\text{CTRL}}$ and $f_{\text{CLOCK}}$
- In the equilibrium condition, $f_{\text{REF}} = f_{\text{FB}}$ and the PLL generates a output frequency $N$ times bigger than $f_{\text{REF}}$
- $V_{\text{UP}}$ and $V_{\text{DN}}$ remains at low level
**Case Study Circuit**

**PLL designed:**
- TSMC 0.35μm CMOS technology
- $f_{\text{CLOCK}} = 500$MHz
- Division rate = 8

**Measured values:**
- $f_{\text{CLOCK}} = 499.96$MHz
- $V_{\text{CTRL}} = 1.6434$V
- $P_{\text{RMS}} = 9.1897$mW
- Lock time $\approx 1$μs
• TID effects are modeled as threshold voltage variations ($\Delta V_{th}$), according to experimental data (Lacoe et al., 1998)

• The standard deviations were obtained from (Paniz, 2010)

• **Note 1:** These data are not specific to TSMC process, but for a commercial HP 0.35µm technology (same L, same tox, close values to doping and mobility)

• 10,000 Spice simulations were performed for each accumulated dose value using the Monte-Carlo method, assuming a gaussian distribution for $\Delta V_{th}$

• **Note 2:** The leakage current contribution on the PLL performance degradation was ignored, since the author did not provide statistical data for this parameter

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**Methodology**

**$V_{TH}$ Shifts**

$V_{TH}$ shifts for 0.35µm PMOS transistors

<table>
<thead>
<tr>
<th>Dose [krad]</th>
<th>$\Delta V_{th,p}$ [mV]</th>
<th>$1\sigma$ [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>-1.5</td>
<td>1.61</td>
</tr>
<tr>
<td>30</td>
<td>-3.6</td>
<td>2.02</td>
</tr>
<tr>
<td>50</td>
<td>-5.6</td>
<td>1.61</td>
</tr>
<tr>
<td>70</td>
<td>-7.9</td>
<td>0.81</td>
</tr>
<tr>
<td>100</td>
<td>-8.0</td>
<td>2.82</td>
</tr>
<tr>
<td>300</td>
<td>-18.7</td>
<td>29.8</td>
</tr>
</tbody>
</table>

$V_{TH}$ shifts for 0.35µm NMOS transistors

<table>
<thead>
<tr>
<th>Dose [krad]</th>
<th>$\Delta V_{th,n}$ [mV]</th>
<th>$1\sigma$ [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>37.2</td>
<td>22.1</td>
</tr>
<tr>
<td>30</td>
<td>42.6</td>
<td>34.4</td>
</tr>
<tr>
<td>50</td>
<td>30.4</td>
<td>23.4</td>
</tr>
<tr>
<td>70</td>
<td>29.3</td>
<td>24.6</td>
</tr>
<tr>
<td>100</td>
<td>29.7</td>
<td>35.7</td>
</tr>
<tr>
<td>300</td>
<td>-60.3</td>
<td>45.4</td>
</tr>
</tbody>
</table>

Lacoe *et. al.* 1998
• For output frequency measurement, a time window containing 200 periods of clock was used

• The frequency was determined as the inverse of the arithmetic average of these periods

• To determine VCO control voltage and RMS power values, the average of these variables was calculated in the same window

• It is important to note that these measurements were carried out in a stable region of operation

\[ f_{\text{CLOCK}} = \frac{200}{T'} \]
Results

Output Frequency

PLL Output Frequency @10krad
\[ \mu_F = 499.84 \text{MHz} \]
\[ \sigma_F = 130.67 \text{kHz} \]

PLL Output Frequency @30krad
\[ \mu_F = 499.75 \text{MHz} \]
\[ \sigma_F = 306.88 \text{kHz} \]

PLL Output Frequency @50krad
\[ \mu_F = 499.84 \text{MHz} \]
\[ \sigma_F = 137.70 \text{kHz} \]

PLL Output Frequency @70krad
\[ \mu_F = 499.83 \text{MHz} \]
\[ \sigma_F = 150.78 \text{kHz} \]

PLL Output Frequency @100krad
\[ \mu_F = 499.76 \text{MHz} \]
\[ \sigma_F = 304.14 \text{kHz} \]

PLL Output Frequency @300krad
\[ \mu_F = 499.86 \text{MHz} \]
\[ \sigma_F = 643.27 \text{kHz} \]
What we observed about PLL output frequency?

- The mean value remains close to each other for all simulated doses
- Large deviation on the output frequency can be observed in the simulations of 30krad and 300krad
- These values was attributed to the increase in the PLL lock time, which affects the stability of output frequency in the measurement window
- For all the simulations, the standard deviation of the output frequency proved to be proportional to the standard deviation of the NMOS threshold voltage shifts
- It was not found correlation between PMOS threshold voltage shifts and these measured data.
## Results

### Control Voltage

- **PLL Control Voltage @10krad**
  - $\mu_V = 1.6849V$
  - $\sigma_V = 13.353mV$

- **PLL Control Voltage @30krad**
  - $\mu_V = 1.6930V$
  - $\sigma_V = 20.903mV$

- **PLL Control Voltage @50krad**
  - $\mu_V = 1.6771V$
  - $\sigma_V = 14.085mV$

- **PLL Control Voltage @70krad**
  - $\mu_V = 1.6761V$
  - $\sigma_V = 14.760mV$

- **PLL Control Voltage @100krad**
  - $\mu_V = 1.6779V$
  - $\sigma_V = 21.485mV$

- **PLL Control Voltage @300krad**
  - $\mu_V = 1.5750V$
  - $\sigma_V = 31.295mV$
What we observed about VCO control voltage?

- The control voltage distribution presented a gaussian distribution.
- VCO control voltage mean value increases when NMOS threshold voltage has a positive shift.
  - Higher $V_{TH}$ = less current for a same $V_{GS}$
  - More voltage ($V_{CTRL}$) is needed to generate the same frequency
- VCO control voltage mean value decreases when NMOS threshold voltage has a negative shift.
  - Lower $V_{TH}$ = more current for a same $V_{GS}$
  - Less voltage ($V_{CTRL}$) is needed to generate the same frequency
- The measured standard deviations in the VCO control voltage is shown proportional to the standard deviation of the NMOS threshold voltage shifts.
Results

RMS Power Consumption

PLL Power Consumption @10krad

\[ \mu_P = 9.2565\text{mW} \]
\[ \sigma_P = 0.7791\text{mW} \]

PLL Power Consumption @30krad

\[ \mu_P = 9.1952\text{mW} \]
\[ \sigma_P = 1.0928\text{mW} \]

PLL Power Consumption @50krad

\[ \mu_P = 9.2495\text{mW} \]
\[ \sigma_P = 0.7776\text{mW} \]

PLL Power Consumption @70krad

\[ \mu_P = 9.2827\text{mW} \]
\[ \sigma_P = 1.3696\text{mW} \]

PLL Power Consumption @100krad

\[ \mu_P = 9.2414\text{mW} \]
\[ \sigma_P = 0.9243\text{mW} \]

PLL Power Consumption @300krad

\[ \mu_P = 9.6186\text{mW} \]
\[ \sigma_P = 2.4725\text{mW} \]
What we observed about the PLL power consumption?

- The PLL showed the highest consumption when the NMOS threshold voltage had a negative shift
- For positive values of NMOS threshold shifts, the consumption is shown inversely proportional to the shifts
  - Larger threshold shift = Less power consumption
- It was not found correlation between PMOS threshold shifts and these measured data.
- **Note 3:** in a practical situation, the current leakage induced by the radiation can increase the PLL power consumption beyond these measured values
Results
PLL Failing Cases

- The PLL presented functional failures when subjected to doses of 30 krad and 300 krad
- The percentage of failures was 0.04%
- In all PLL failing cases, the problem was originated at the first stage of frequency divider
- The mechanism of the failures was not clearly identified
Conclusions

• The PLL performance is affected negatively by the radiation, causing:
  • Power consumption increase
  • Output frequency shifts
  • Functional failures
• NMOS threshold voltage shifts have greater impact in the circuit performance than PMOS threshold voltage shifts
• Although not considered in the simulations, it is expected that the leakage current contribute only as an increase in power consumption
• Future work:
  • Perform simulations considering the current leakage contribution (experimental results are needed)
Thank you!

Alan Carlos Junior Rossetto
Microelectronics Program – PGMICRO/UFRGS
alan.rossetto@inf.ufrgs.br

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