LATW 2014
15th IEEE Latin-American Test Workshop
PRELIMINAR TECHNICAL PROGRAM
Fortaleza, Brazil, March 12th - 15th, 2014
15th IEEE Latin-American Test Workshop
PRELIMINARY TECHNICAL PROGRAM

Wednesday, 12th March 2014

08:00 - 08:30  Registration

08:30 - 09:00  Opening Session

09:00 - 09:40  KEYNOTE  
Title: TBD  
Presenter: TBD

09:40 - 10:10  COFFEE BREAK

10:10 - 11:10  SESSION 01: DESIGN VERIFICATION AND VALIDATION  
Session Chair: TBD

ON THE REUSE OF RTL ASSERTIONS IN SYSTEMC TLM VERIFICATION  
Nicola BOMBIERI, Franco FUMMI, Valerio GUARNIERI, Graziano PRAVADELLI,  
Francesco STEFANINI, Tara GHASEMPOURI, Michele LORA, Giovanni AUDITORE,  
Mirella NEGRO MARCIGAGLIA

SIMPLIFIED STIMULI GENERATION FOR SCENARIO AND  
ASSERTION BASED VERIFICATION  
Graziano PRAVADELLI, Luca PICCOLBONI

A UNIFIED SEQUENTIAL EQUIVALENCE CHECKING APPROACH TO VERIFY HIGH-LEVEL  
FUNCTIONALITY AND PROTOCOL SPECIFICATION IMPLEMENTATIONS IN RTL DESIGNS  
Carlos Ivan CASTRO MARQUEZ, Marius STRUM, Wang CHAU

11:10 - 12:30  SESSION 02: FAULT MODELING AND SIMULATION  
Session Chair: TBD

SEU FAULT-INJECTION AT SYSTEM LEVEL: METHOD, TOOLS AND  
PRELIMINARY RESULTS  
Wassim MANSOUR, Pablo RAMOS, Rafic AYOUBI, Raoul VELAZCO

ANALYSIS OF THE EFFECTS OF SINGLE EVENT TRANSIENTS ON AN SAR-ADC  
BASED ON CHARGE REDISTRIBUTION  
Alisson LANOT, Tiago BALEN

POSSIBILITIES OF DEFECT-SIZE MAGNIFICATION FOR TESTING RESISTIVE-OPENS  
IN NANOMETER TECHNOLOGIES  
Jose GARCIA-GERVACIO, Jaime MARTINEZ, Victor CHAMPAC

SOFTWARE ERROR INJECTION METHODOLOGY BASED ON QEMU SOFTWARE PLATFORM  
Filibre GEISSLER, Fernanda KASTENSMIDT
15th IEEE Latin-American Test Workshop
PRELIMINARY TECHNICAL PROGRAM

Wednesday, 12th March 2014

12:30 - 14:00  LUNCH

14:00 - 14:40  INVITED TALK
Title: IC Reliable and Quality Challenges and Forthcomming Technology Nodes
Presenter: Said HAMDIOUI, Delft University of Technology, Netherlands

14:40 - 15:40  SESSION 03: FAULT TOLERANT ARCHITECTURES
Session Chair: TBD

DESIGN DIVERSITY REDUNDANCY WITH SPATIAL-TEMPORAL VOTING
APPLIED TO DATA ACQUISITION SYSTEMS
Cristiano CHENET, Tiago BALEN, Alisson LANOT
Federal University of Rio Grande do Sul (UFRGS), Brazil

IMPROVING THE ROBUSTNESS OF A SWITCH BOX IN A MESH OF CLUSTERS FPGA
Arwa BEN DHIA, Mariem SLIMANI, Lirida NAVINER
Institut TELECOM, TELECOM ParisTech, LTCI-CNRS France

FAULT TOLERANCE EVALUATION OF RFID TAGS
Omar ABDELMALEK, David HELY, Vincent BEROULLE

15:40 - 16:10  COFFEE BREAK

16:10 - 17:30  SESSION 04: FAULT TOLERANCE IN HARDWARE AND SOFTWARE
Session Chair: TBD

FAULT TOLERANT LINEAR STATE MACHINES
Stefan WEIDLING, Michael GOESSEL
University of Potsdam, Germany

IDSM: AN IMPROVED DISJOINT SIGNATURE MONITORING SCHEME
FOR PROCESSOR BEHAVIORAL CHECKING
Salma BERGAOUI, Pierre VANHAUWAERT, Regis LEVEUGLE

METHODOLOGY FOR ACHIEVING BEST TRADE-OFF OF AREA AND
FAULT MASKING COVERAGE IN ATMFS
Iuri GOMES, Mayler MARTINS, Fernanda KASTENSMIDT, André REIS, Sylvain NOVALÈS

ON RELIABILITY ENHANCEMENT USING ADAPTIVE CORE VOLTAGE SCALING AND VARI-
ATIONS ON 28NM LOW-POWER PROCESS FPGAS
Petr PFEIFER, Zdenek PLIVA

19:00  WELCOME COCKTAIL
CEITEC Master’s Thesis Award – Ceremony
15th IEEE Latin-American Test Workshop
PRELIMINARY TECHNICAL PROGRAM

Thursday, 13th March 2014

09:00 - 10:20  SPECIAL SESSION 01
Title: Analog Mixed Signal Test
Organizer: Florence AZAIS - LIRMM, France

SPECIFICATION TEST MINIMIZATION FOR GIVEN DEFECT LEVEL
Suraj SINDIA, Vishwani AGRAWAL

HARMONIC DISTORTION CORRECTION FOR 8-BIT DELAY LINE ADC USING GRAY CODE
Hsun-Cheng LEE, Jacob ABRAHAM

EVALUATION OF INDIRECT MEASUREMENT SELECTION STRATEGIES IN THE CONTEXT OF ANALOG/RF ALTERNATE TESTING
Syhem LARGUECH, Florence AZAIS, Serge BERNARD, Mariane COMTE, Vincent KERZERHO, Michel RENOVELL

DEVELOPMENT OF A DIGITAL TOOL FOR THE SIMULATION OF A READOUT SYSTEM DEDICATED FOR NEUTRON DISCRIMINATION
Sabrine BEN KRIT, Wenceslas RAHAJANDRAIBE, Karine COULIE-CASTELLANI

10:20 - 10:50  COFFEE BREAK

10:50 - 11:30  SPECIAL SESSION 02:
Title: Test and Reliability of Embedded Systems based on WSNs
Organizer: Cesar Augusto MISSIO MARCON - Catholic University of Rio Grande do Sul, Brazil:

A NOVEL CONTROL STRATEGY FOR FAIL-SAFE CYCLIC DATA EXCHANGE IN WIRELESS SENSOR NETWORKS
Pablo BRIFF*, Ariel LUTENBERG*, Leonardo REY VEGA*, Fabian VARGAS**, Mohammad PATWARY*

*Universidad de Buenos Aires, Argentina
**Catholic University of Rio Grande do Sul (PUCRS), Brazil
Thursday, 13th March 2014

11:30 - 12:00  SESSION 09: PROJECT IN PROGRESS
Session Chair: TBD

THE IEEE STD 1149.6-2003 OVERVIEW
Francisco RUSSI
Synopsys, USA

12:00 - 13:30  LUNCH

13:30 - 14:10  SESSION 05: DIAGNOSIS AND BUILT-IN SELF TEST
Session Chair: TBD

IMPLEMENTATION AND EXPERIMENTAL EVALUATION OF A CUDA CORE UNDER SINGLE EVENT EFFECTS
Jose Rodrigo AZAMBUJA, Werner NEDEL, Fernanda KASTENSMIDT

LOW COST FAULT DETECTOR GUIDED BY PERMANENT FAULTS AT THE END OF FPGAS LIFE CYCLE
Victor MARTINS, Frederico FERLINI, Djones LETTNIN, Eduardo BEZERRA

SOCIAL EVENT
Boat Trip
Gala Dinner
Friday, 14th March 2014

08:30 - 09:50  SESSION 06: RADIATION AND ELECTROMAGNETIC INTERFERENCE
Session Chair: TBD

IMPROVEMENT OF A VCO CONCEPT FOR LOW ENERGY PARTICLE DETECTION AND RECOGNITION
Karine COULIE-CASTELLANI, Wenceslas RAHAJANDRAIBE, Gilles NICOLAU, Hassen AZIZA, Jean Michel PORTAL

THE EFFECTS OF TOTAL IONIZING DOSE ON THE NEUTRON SEU CROSS SECTION OF A 130 NM 4 MB SRAM MEMORY
Odair GONCALEZ, Evaldo C. F. PEREIRA JUNIOR, Rafael VAZ, Claudio FEDERICO, Gilson WIRTH, Thiago BOTH

SOFT ERROR RATE IN SRAM-BASED FPGAS UNDER NEUTRON-INDUCED AND TID EFFECTS
Lucas TAMBARA, Jorge TONFAT, Ricardo REIS, Fernanda KASTENSMIDT, Evaldo C. F. PEREIRA JUNIOR, Rafael VAZ, Odair GONCALEZ

PERFORMANCE ANALYSIS OF A CLOCK GENERATOR PLL UNDER TID EFFECTS
Alan ROSSETTO, Gilson WIRTH, Ricardo DALLASEN

09:10 - 10:30  INVITED TALK
Title: Design of On-Chip Sensors to Monitor Electromagnetic Activity in ICs: Towards Online Diagnosis and Self-Healing
Presenter: Sonia BEN DHIA, LAAS/INSA, Toulouse, France

10:30 - 11:00  COFFEE BREAK

11:00 - 12:00  PANEL
Title: Regaining Hardware Trust: Security Challenges during Reliable System Design
Panelists: David HELY, Jennifer DWORAK, Ozgur SINANOGLU, Ramesh KARRI

12:00 - 13:00  LUNCH

13:00 - 14:30  PANEL
Title: Radiation Facilities in South America and Expected Reliability for Space Applications
Organizers: Raoul VELAZCO, Fernanda KASTENSMIDT
Panelists: Vincent POUGET, Claudio FEDERICO, Silvio MANEA, José LIPOVETZKY, Pablo FERREYRA, Juan FRAIRE
15th IEEE Latin-American Test Workshop
PRELIMINARY TECHNICAL PROGRAM

Friday, 14th March 2014

14:30 - 15:10  INVITED TALK
Recent Progress of Software-Related Electromagnetic Interference
Shih-Yi YUAN
Feng Chia University, Taiwan

15:10 - 15:40  COFFEE BREAK

15:40 - 16:40  SESSION 07: SOFTWARE FAULT-TOLERANCE AND TESTING
Session Chair: TBD

OPTIMIZED HYBRID VERIFICATION OF EMBEDDED SOFTWARE
Joerg BEHREND, Alexander GRUENHAGE, Douglas SCHROEDER, Djones LETTNIN,
Juergen RUF, Thomas KROPF, WOLFGANG ROSENSTIEL

EFFICIENT METRIC FOR REGISTER FILE CRITICALITY IN PROCESSOR-BASED SYSTEMS
Felipe RESTREPO-CALLE, Sergio CUENCA-ASENSI, Antonio MARTÍNEZ-ÁLVAREZ,
Eduardo CHIELLE, Fernanda KASTENSMIDT

SOFTWARE-BASED SELF-TEST GENERATION FOR MICROPROCESSORS WITH
HIGH-LEVEL DECISION DIAGRAMS
Raimund UBAR, Anton TSERTOV, Artjom JASNETSKI, Marina BRIK

16:40 - 17:40  SESSION 08: HARDENING TECHNIQUES
Session Chair: TBD

REDUCING SEU SENSITIVITY IN LIN NETWORKS: SELECTIVE AND COLLABORATIVE
HARDENING TECHNIQUES
Anna VASKOVA, Fabregat AROA, Marta PORTELA-GARCIA, Mario GARCIA-VALDERAS, Celia
LOPEZ-ONGIL, Matteo SONZA REORDA

SCHMITT TRIGGER ON OUTPUT INVERTERS OF NCL GATES FOR SOFT ERROR
HARDENING: IS IT ENOUGH?
Matheus MOREIRA, Ricardo GUZZELLI, Ney CALAZANS

HIERARCHICAL IDENTIFICATION OF NBTI-CRITICAL GATES IN NANOSCALE LOGIC
Jaan RAIK, Sergei KOSTIN, Maksim JENIHHIN, Raimund UBAR, Fabian VARGAS

17:40 - 18:10  CLOSING REMARKS
Saturday, 15th March 2014

10:00 - 12:30  ROUND TABLE:
Title: Prospecting Collaborations with Latin American Universities
Presenter: Fabian VARGAS - Catholic University of Rio Grande do Sul, Brazil
Saturday, 15th March 2014